REMARKS

Claims 1-37 are pending, with claims 13 and 16-37 rejected, and claims 1-12, 14, and 15 withdrawn from consideration. Claims 38-41 have been added.

Claims 13 and 16-27 have been rejected under 35 USC 112, second paragraph, as being indefinite. The Examiner questions the relations among some of the calimed elements.

The "partial sum table" in the master control unit is allocated, as an example, on a per searcher basis to extend search control flexibility across time slots. (See paragraph [0023].)

The "data caches" are also used for caching intermediate data which could be the intermediate data when complete process is carried out over more than one time slot. (See paragraph [0024], where it describes that the data cache can be built as multi-port RAM accessible by all signal processing elements.) As understood by a person of ordinary skill in the art, each signal processing element can read and write to the data cache. The signal processing elements can therefore store intermediate data at the end of a time slot to the data cache and read the intermediate data at the beginning of a time slot in order to continue the unfinished processing function.

In view of the above, Applicant respectfully submits that the claims are definite. Reconsideration and withdrawal of the 112 rejection is respectfully requested.

Claims 13 and 16-37 have been rejected under 35 USC 103 (a) as being unpatentable over Belotserkovsky et al. (U.S. Patent No. 6,621,857; "Belotserkovsky") in view of Schuster et al. (U.S. Patent No. 6,591,355; "Schuster"). Applicant respectfully traverses this rejection.

The applied references do not suggest a "partial sum table," as required by the claimed invention.

The claimed time-sliced signal processor requires that the signal processing for a particular transceiver is carried out only during its assigned time slice. If the complete processing operation requires more than one time slice, a time sliced processor needs to store sufficient processor date (i.e., state information and intermediate results) at the end of a time slice in order to continue the unfinished processing at the beginning of the next assigned time slice. While a complete processing operation is performed in multiple time slices, it is further required that the final results are identical to the ones that are obtained when the processing operation is carried out continuously from start to complete. It is also well known that maintaining chip rate synchronization is critical to the correct operation of spread spectrum systems, and a spread spectrum transceiver must be designed to maintain such synchronization irrespective of what architecture is used. The claimed time-sliced processor was designed specifically to fulfill the above requirements. The size of a time slice is independent of communication protocols and is a parameter available for optimizing other design criteria, such as power consumption, silicon area, etc.

On the other hand, Belotserkovsky's TDMA transceiver operates on TDMA time slot basis. To a person having ordinary skill in the art, it is understood that a complete processing operation of a TDMA slot is from the beginning of the slot to the end of the same time slot. Belotserkovsky's TDMA transceiver starts its operation at the beginning of its assigned TDMA time slot and continues to finish the operation at the end of the same time slot. As a result, it would not be reasonable for such a transceiver to include any modules or components or mechanisms for storing and recovering intermediate results and state according to the requirements for a time-sliced processor as described

in the previous paragraph. Additionally, the size of a time slot in Belotserkovsky is a design specification dictated by the communication protocol.

The architecture according to Schuster is designed for adjust the granularity for shared memory access. It is obvious that such architecture is not suitable for adjusting processing time allocation as required by a time-sliced based signal processing method since they are two different design issues.

The claims are therefore patentable over the applied references for at least these reasons.

In view of the above, Applicant believes the pending application is in condition for allowance.

Dated: December 18, 2006

Respectfully submitted,

By /Laura C. Brutman/
Laura C. Brutman
Registration No.: 38,395
DICKSTEIN SHAPIRO LLP
1177 Avenue of the Americas
41st Floor
New York, New York 10036-2714
(212) 277-6500
Attorney for Applicant